Wenqi Yin

Mobile Phone	(512)-865-8089	**Address**	2501 Speedway EERC, Austin TX 78712
Email	wqyin@utexas.edu	**Github**	https://github.com/SleepBook

Education

Sep 2017 - Present **PhD Student in Computer Engineering**
Advised by Professor Mattan Erez, The University of Texas at Austin

Sep 2012 - Jun 2016 **B.Eng in Electrical Engineering**
Shanghai Jiao Tong University

Experience

Jun 2019 - Aug 2019 **Intern**
Xilinx Research Lab
FPGA TCP Parser, Hyperledger Fabric

May 2018 - Aug 2018 **Intern**
Synopsys Inc.
SIMD Unit Cache Modelling for ARC Processors

Sep 2016 - Dec 2018 **Teaching Assistant**
Univ. of Texas at Austin, Shanghai Jiao Tong Univ.
EE312 Software Design and Implementation I(C, C++), EE422C Software Design and Implementation II(Java), CS427 GPGPU Computing

Publication

- Chun-Kai Chang, Wenqi Yin, and Mattan Erez. Assessing The Impact of Timing Errors on HPC Applications. In the Proceedings of the ACM/IEEE International Conference on High-Performance Computing, Networking, Storage, and Analysis (SC19). 2019

- Chengwen Xu, Xiangyu Wu, Wenqi Yin, Qiang Xu, Naifeng Jing, Xiaoyao Liang and Li Jiang, "On Quality Trade-off Control for Approximate Computing using Iterative Training" ACM/IEEE Design Automation Conference (DAC), June. 2017

Selected Projects

Jan 2020 - Present **Performance QoS Support in Memory Subsystem**
Explore and evaluate Hardware based resource management mechanism for performance QoS in memory subsystem

Oct 2018 - Dec 2019 **Microprocessor Fault Injection**
Design and implement a FPGA-based platform for injecting faults into microarchitectural states of microprocessor

Sep 2018 - Nov 2018 **VLSI Design Labs**
4-bit SRAM cell layout, achieved area of 6.58μm^2 with 45nm technology. Gate Level 16-bit ALU design. Behavior level Synchronous Serial Port Module design and Integration with Wishbone interface

Feb 2018 - Apr 2018 **FPGA Accelerator Design and Implementation for PageRank Algorithm**
Design and implement a page rank accelerator on Xilinx Zynq FPGA, including the HW circuit design and Linux driver development

Sep 2016 **SPICE Circuit Simulator Development**
Developed a netlist circuit simulator in Python. Project hosted at https://github.com/SleepBook/pySpice

Mar 2016 - Jun 2016 **GPU Acceleration for CNN on Mobile Devices**
Using GPUs in mobile SOCs for accelerating CNN Lenet inference. Work includes implementing and optimizing the neural network using OpenCL and deploying it on several major SOC platforms.

Skills

Programming C/C++ Python Java Verilog HDL Chisel HDL Go

Software & Tools Gem5 Xilinx FPGA Tools CUDA/OpenCL RISC-V Rocketchip/BOOM Regent/Legion

Related Coursework

UT Austin Computer Architecture, Advanced Operating System, Algorithm, Advanced Microcontroller, VLSI, Parellel Computing, Data Center, Probablity and Stochastic Process

SJTU Computer Organization, Operating System, Digital Circuit Design, Analog Circuit Design, Electronic Design Automation, Multicore Architecture and Parallel Computing, Communication System